Remarks

Claims 17 and 20 are amended for improved clarity. Claims 1 - 21 are in the Application, of which claims 1 - 13 were withdrawn as being drawn to a nonelected invention. Claims 14 - 21 are under consideration. Reconsideration of the Application, as amended, is requested.

The Application describes metallurgic connection between bumps on a chip and interconnection points on a substrate metallization, and methods for making the connection. The bumps are preferably gold stud bumps, and the interconnection points are preferably tin spots formed on the metallization. The gold stud bumps are contacted with the tin spots, and heat is applied to a temperature and for a time sufficient to give a metallurgical reaction at the interface between the bumps and the spots. For a gold-tin junction, a suitable temperature is about 232 °C, and a suitable time is one to two seconds. At about 232 °C, the tin spots melt and the temperature at the bonding interface increases significantly, thereby dissolving some gold from the stud bumps to create a bonding phase at the interface between the substrate metallization and the gold stud bumps. Because the temperature is raised only for a short period of time, the bonding phase is limited to a thin layer at the interface between the metallization and the gold stud bumps.

The points raised by the Examiner will now be addressed, beginning with the rejection under 35 U.S.C. § 102.

Rejection under 35 U.S.C. § 102

Claims 14 and 16 were rejected under 35 U.S.C. § 102(b) as being anticipated by Scharr *et al.* U.S. 5,346,857 ("Scharr"). The Examiner asserted:

> Scharr et al. (figure 2) teach a chip (26) having bumps (28) formed thereon and a substrate (21) having interconnect points on a metallization (23) thereon, the bumps (28) forming contacts with the interconnect points, wherein each the contact comprises an interconnection layer situated at an interface between the bump (28) and the interconnect point (metallization layer [23]) in contact therewith, the layer comprising an alloy (a region indicated by line [29]) of the material of the bump (28) and the material of the metallization (23) (see figure 2; column 3, line 54 – column 4, line 16).
>
> Regarding claim 16, Scharr et al. teach the bump (28) material comprises gold and the interconnect points (metallization [23]) comprise Sn, and the alloy (a region indicated by line [29]) at the interface comprises a Au/Sn alloy (see figure 2; column 3, line 54 – column 4, line 16).

These rejections are substantially the same as in the previous Office action.

As to Applicants' earlier arguments that Scharr does not teach or suggest the limitations of claim 14, the Examiner stated that the arguments were not convincing, and substantially repeated his earlier assertions.

These rejections are again traversed.

The Office action states, with reference to Scharr Figure 2, that Scharr "teaches ... an interconnection layer situated at an interface between the bump (28) and the interconnect point (metallization layer [23]) in contact therewith, the layer comprising an alloy (a region indicated by line [29]) of the material of the bump (28) and the material of the metallization (23) ..." To the extent this may be understood, Applicants disagree with this interpretation of Scharr and, particularly, with this interpretation of what "line 29" shows, and this interpretation of "interconnect point". Scharr states at Col. 3, lines 56 - 65 (emphasis added):

> Flip-chip bonded structure **20** includes a substrate **21** having a plurality of bonding areas on a major surface. The bonding areas may be, for example, copper **22** coated with tin **23**. ... Gold bumps **28** are brought into contact with tin **23**. Pressure and heat are applied to the structure as described in FIG. **1** thereby forming a gold-tin eutectic alloy in the regions indicated by lines **29**.

The "lines **29**" are double-headed arrows. The tips of each arrow touch thin vertical lines that reach to the edges of the area of contact of the bump **28** with the surface of the tin **23**. That is, the "lines **29**" appear to show the width of the area of contact of the bump and the tin surface **23**; the "lines **29**" are said by Scharr to "indicate" "regions" in which the gold-tin eutectic alloy is formed.

Whatever may be shown by "lines **29**", the "lines **29**" in Scharr FIG. **2** do not show an interconnection layer situated at an interface between the bump and the interconnect point in contact therewith, the layer comprising an alloy of the material of the bump and the material of the interconnect point" as recited in claim 14 of the Application. Whatever the "regions indicated by lines **29**" may be, Scharr does not show or describe an interconnection layer at the interface between the bump (such as gold) and the interconnect point (such as tin).

There are no lines in Scharr FIG. **2** showing a layer at an interface between the gold bump **28** and the tin **23**.

Nor can such a layer be suggested in Scharr, because, as explained below the alloyed region resulting from the method of Scharr will constitute a substantial portion of the bump.

In further factual support of Applicants' arguments, reference is made to a phase diagram of the gold-tin system, attached as Appendix A ("Constitution of Binary Alloys", M. Hanson, 2d Ed., McGraw Hill, 1958 pp.232-233) (the "phase diagram"). The phase diagram shows liquidus and solidus lines for a range of percents of Au and Sn, from 100% Au at the left extreme, and 100% Sn at the right extreme, and a range of temperatures, from 100 °C. to 1100 °C.

The melting temperature of pure Tin is 232 °C. This is shown in the phase diagram by the intersection of liquidus line with the ordinate at the right extreme of the diagram. (The "liquidus line" is the line on a phase diagram above which the composition is liquid; the "solidus line" is the line on a phase diagram below which the composition is solid).

The phase diagram also shows a solidus line for a gold-tin eutectic at 217 °C.
For a Au-Sn junction, according to Applicants' invention a suitable temperature is about 232° C. and a suitable time is 1-2 seconds. At that temperature the Sn spots melt and, according to Applicants' specification, "the temperature at the bonding interface increases significantly, thereby dissolving some Au ... to create a bonding phase at the interface ... Preferably a 80%:20% Au:Sn alloy is formed at the interface". Applicants' Fig. 1B clearly shows that the bonding phase (alloy) is limited to a layer 26 at the interface of the bump and the interconnect point. The remainder of the bump is left substantially undisturbed by the process, and the bumps serve to maintain a standoff height between the die and the substrate during the bonding process.

According to the method described in the Application, the die is heated, raising the temperature of the gold bumps. Upon contact of a gold bump with a tin spot, the tin is rapidly heated by the bump, melting at about 232 °C., and gold begins to diffuse into the tin from the bump. As gold diffuses across the gold/tin interface into the molten tin, gold-tin intermetallics form (principally $AuSn_4$). As diffusion of gold into the tin continues, the gold-tin composition becomes progressively less tin rich over time, forming one gold-tin intermetallic or another (such

as $AuSn_4$ and $AuSn_2$), and the composition solidifies. At this point, there is no more liquid phase in the system, and any further reaction substantially stops, forming the bonding phase at the interface between the gold bump and the interconnect point. This process is complete within 2 seconds' time.

Because the proportion of gold is low (less than 20 %) in the bonding phase according to the Application, and because the density of the bonding phase is greater than the density of pure tin, the bonding phase will be confined to a thin layer at the interface between the bump and the interconnect point.

In contrast, the Scharr process applies significantly higher heat for a significantly longer time, and Scharr expressly teaches that temperatures below approximately 280° C. are ineffective (Col. 3, lines 33 - 35).

According to the method described in Scharr, the die and substrate are brought into contact, and then the circuit board (the substrate) is heated to a temperature in the range 280 °C. to 315 °C., and pressure is applied. The phase diagram shows a solidus line for a gold-tin eutectic at 280 °C., for a composition about 80:10 Au:Sn. In the Scharr method, the tin melts, and rapidly incorporates gold. The tin will continue to dissolve gold so long as some liquid phase is present in the system, until the nominal 80:20 Au:Sn composition is reached. According to Scharr, this process requires a time in excess of 3 to 10 seconds.

Because according to the method of Scharr, the bonding temperature exceeds the solidus temperature for his nominal composition (80:20 Au:Sn), the composition will be molten at the bonding temperature, and the desired eutectic is formed by freezing, as the temperature is eventually lowered. Hence a homogeneous alloy of the nominal composition 80:20 Au:Sn forms under those bonding conditions.

Because in Scharr the proportion of gold is high (nominally 80 %) in the alloyed region, the alloyed region will not be a thin layer. Instead, the alloyed region would be expected to constitute a substantial portion of the bump, and indeed the alloyed region could make up the entire bump.

Moreover, Scharr describes applying a compression load ranging between approximately 3 and 5 g per bump, for a time in excess of a range between 3 and 10 seconds. Because the heater is turned on prior to applying the load, and is turned off following the load period, Scharr teaches maintaining the high temperature régime for a time in excess of 3 to 10 seconds.

The temperature régime described by Scharr promotes bulk melting of the Au-Sn eutectic composition and alloy formation in the bulk of the bump, and can result in uncontrolled collapse of the bumps and degradation of the standoff height between die and substrate.

Accordingly, whatever may be meant by the "lines 29", Scharr does not teach an alloy layer formed at an interface between the bump and the material of the interconnect point, as in Applicants' invention as claimed.

Moreover, far from suggesting such a structure, Scharr expressly teaches that a process for forming such a structure, as described in Applicants specification, will be ineffective to form an alloy as described by Scharr.

Accordingly, Scharr neither teaches nor suggests these features of applicants' invention, and the rejection for anticipation by Scharr should be withdrawn.

Rejections under 35 U.S.C. § 103(a)

Claims 15 and 18 - 20 were rejected under 35 U.S.C. § 103(a) for obviousness over Scharr in view of Nakamura *et al.* U.S. 6,326,234 ("Nakamura"). The Examiner acknowledged that Scharr does "not teach a cured adhesive polymer is situated in a middle region between the bump surface of the chip and the surface of the substrate", but asserted (referring to Nakamura figure 4) that "Nakamura teaches an adhesive polymer (7) is situated in a middle region between the bump surface of the chip (1) and the surface of the substrate (2)", and argued that it would have been obvious:

> to incorporate the teaching of Nakamura into the device taught by Scharr et al., because it provides good adhesion between the chip and the substrate.

This rejection is traversed. As explained above, Scharr does not teach the alloy layer according to Applicants' invention as claimed; and Nakamura cannot supply what Scharr lacks.

Moreover, the Examiner has not addressed the following explanation, made in Applicants' earlier response: Applicants' claims recite a cured adhesive polymer (that is, a curable polymer

that has been cured in the claimed structure) Nakamura describes (*see*, Nakamura Fig. 4) a semiconductor device 10 in which the center of the gap 11 between the semiconductor chip 1 and the circuit board 2 is adhesively filled with a thermoplastic resin 7; and in which a peripheral portion of the chip is sealed by a curable resin 5 such as photocurable or thermosetting resin to form the semiconductor device 10. The thermoplastic resin works not to establish "good adhesion", but to provide for subsequent removal of the chip if the resulting assembly tests defective. Thus, it is essential in Nakamura that a thermoplastic resin be used in the center of the gap, as distinguished from a curable resin (Nakamura Col. 4, line 62 - Col. 5, line 12):

> In the conventional face-down type semiconductor device, the semiconductor chip and the circuit board are adhesively attached to each other and electrically coupled to each other by hardening the resin which is put between the semiconductor chip and the circuit board. Accordingly, since the curable resin is used, it is difficult to remove the semiconductor chip when the semiconductor chip is afterwards judged as a defective. However, according to the semiconductor device and the semiconductor device manufacturing method of the present invention, thermoplastic resin is used as temporarily fixing resin, and it is melted to temporarily couple the semiconductor chip and the circuit board to each other. When the semiconductor chip is judged as a defective in a subsequent check test, the semiconductor chip is heated to a temperature which is higher than the melting point or more of the thermoplastic resin to thereby easily remove the defective semiconductor chip from the circuit board.

Thus, Nakamura teaches away from using a curable resin in the center portion of the gap.

Applicants' claim 15 recites that a cured adhesive polymer is situated in a middle region between the bump surface of the chip and the surface of the substrate. No combination of Scharr and Nakamura teaches or suggests Applicants' invention and, accordingly, this rejection for obviousness should be withdrawn.

Claim 17 was rejected under 35 U.S.C. § 103(a) for obviousness over Scharr, the Examiner acknowledging that Scharr does "not explicitly teach the alloy at the interface is 20:80 Sn:Au alloy", but argues that it would have been obvious:

> for an alloy at the interface [to be] 20:80 Sn/Au alloy, says it has been held that discovering an optimum value of the results effective variable involves only routine skill in the art."

(citing *In re Boesch.*)

This rejection is traversed. Applicants have shown how to make an interconnect in which a low temperature and low pressure process is employed to obtain an alloy at the interface between the bumps and the interconnect points. As explained above, Scharr does not teach the alloy layer at the interface according to Applicants' invention as claimed. Moreover, Scharr expressly teaches away from attempting to make a Sn:Au eutectic using a temperature regime as taught by Applicants for making the alloy layer. In other words, no teaching or suggestion of Scharr can make a Sn/Au alloy (in any ratio) limited to a layer at the interface, because Scharr expressly teaches away from using a temperature regime by which such a structure can be obtained according to Applicants' invention.

Accordingly, it is submitted that neither Scharr nor Nakamura—nor any combination of Scharr and Nakamura—makes Applicants' invention. Accordingly, the rejections for obviousness should be withdrawn.

Claim 21 was rejected under 35 U.S.C. § 103(a) for obviousness over Scharr (and Nakamura?) in view of Suzuki *et al.* U.S. 5,997,633 ("Suzuki"). The Examiner acknowledged that Scharr and Nakamura do not show the adhesive polymer forming an underfill, but asserts that Suzuki (figure 14) "teach the adhesive polymer forming an underfill (1010)." This rejection is traversed.

Applicants' claim 18 recites "a first cured adhesive polymer forming a spot situated in a middle region between the bump surface of the chip and the surface of the substrate, there being no first cured adhesive polymer at the contacts" (*see also*, Applicants' paragraph [0014]), and claim 21 recites "further comprising a second cured adhesive polymer forming an underfill." As explained above, no combination of Scharr and Nakamura describes or suggests the first cured adhesive polymer forming a spot situated in a middle region between the bump surface of the chip and the surface of the substrate and not extending to the contacts. Suzuki shows only one polymer forming the underfill **1010**, so it cannot be a "second polymer forming an underfill"; and the underfill **1010** is formed in Suzuki following formation of the electrical contacts (see, Suzuki Col. 2, lines 23 - 25) -- that is, by inflow from between the chip edge and the substrate -- and it must necessarily therefore be at the contacts, so it cannot be the first polymer.

Accordingly, no combination of Scharr and Nakamura and Suzuki makes Applicants' claimed invention, and this rejection for obviousness should be withdrawn.

In view of the foregoing, it is believed that all the claims in the application are in condition for allowance, and action to that effect is requested.

This response is being filed, together with a Request for Continuing Prosecution, within the third month following the shortened statutory period set by the Examiner and, accordingly, it is accompanied by a petition for three months' extension of time and a fee or fee authorization therefor. The Commissioner is authorized to charge any additional fee[s] that may be required in connection with the filing of this paper, or to credit any overpayment, to Deposit Account 50-0869 (Order No. CPAC 1002-1).

If the Examiner determines that a conference would facilitate prosecution of this application, the Examiner is invited to telephone Applicants' representative, undersigned, at the telephone number set out below.

Respectfully submitted,

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Appendix A

"Constitution of Binary Alloys", M. Hanson, 2d Ed., McGraw Hill, 1958 pp.232-233

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Editor

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Metallography

CONSTITUTION OF BINARY ALLOYS

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emf measurements [10]. $AuSn_4$, however, could not be detected by this method, apparently because of the disturbance of equilibrium in the crystallization of alloys with 60–80 wt. % Sn [11].

By powder-pattern X-ray analysis another intermediate phase (ζ) was found which is homogeneous between about 12 and 16 at. (7.5 and 10.3 wt.) % Sn [12].

The boundary of the gold-rich primary solid solution between 388 and 718°C was determined by very careful X-ray analysis [13]. The maximum solubility was

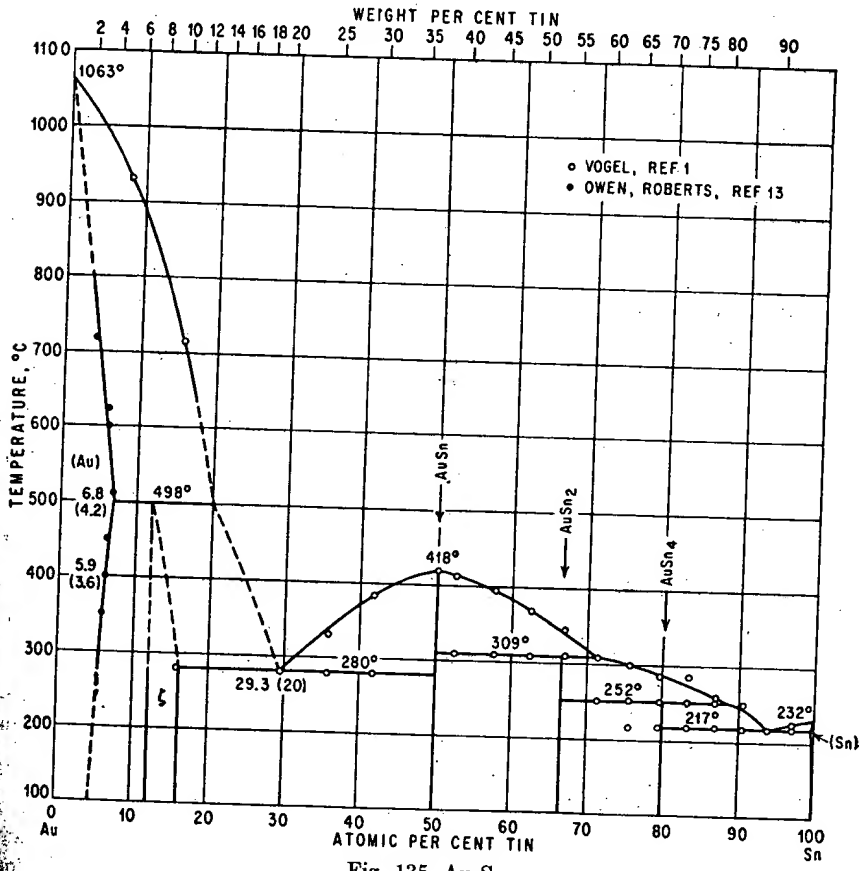

Fig. 135. Au-Sn

found to be 6.8_5 at. (4.2 wt.) % Sn at 498 ± 10°C. At 450, 400, and 350°C solubilities are 6.3_0, 5.9_4, and 5.6_6 at. (3.9, 3.6, and 3.5 wt.) % Sn, respectively. Some observations indicate the temperature of maximum solubility (about 500°C) to be that of the peritectic reaction liq. + (Au) ⇄ ζ. Solubilities above 500°C (Fig. 135) do not claim to be very accurate.

The solid solubility of Au in Sn at 200°C was found by various indirect methods to be about 0.2 at. (0.3 wt.) % Au [14].

Crystal Structures. Lattice parameters of the (Au) phase were determined by [13]. The ζ phase has a h.c.p. structure with probably statistical atom distribution (A3 type) and with $a = 2.90-2.94$ A, $c = 4.78-4.76$ A, $c/a = 1.65-1.62$ [12]. AuSn